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plifying the process. A conductive layer may also be applied to the bottom of substrate 100 (after optional treatment by grinding, etching, implanting, etc.) to form the drain electrode 111.

Note that while source electrode 109 is shown extending 5 down to P-body 107 in the cross-sectional view of FIG. 5K, in other embodiments electrode may only extend to the upper surface of source region 105. It should also be appreciated that electrode 109 does not separate region 105 into two separate source regions in the illustration of FIG. 10 5K. Rather, electrode 109 is fabricated in the form of a plug that is surrounded by N+ material that comprises region 105.

I claim:

1. A method for fabricating a high-voltage transistor comprising:

forming, in a semiconductor substrate of a first conductivity type, first and second trenches that define a mesa having respective first and second sidewalls;

partially filling each of the trenches with a dielectric material that covers the first and second sidewalls:

filling a remaining portion of the trenches with a conductive material to form first and second field plates in the first and second trenches, respectively, the first and second field plates extending vertically from near a bottom of the mesa to a top surface of the semicon- 25 ductor substrate;

forming source and body regions in an upper portion of the mesa, the source region being of the first conductivity type and the body region being of a second conductivity type opposite to the first conductivity 30 type, the body region separating the source from a lower portion of the mesa, the lower portion of the mesa comprising a drift region; and

forming a gate embedded within the dielectric material adjacent the body region, the gate being insulated from 35 the body region and the first and second field plates.

2. The method of claim 1 further comprising;

forming a drain region of the first conductivity type at the bottom of the mesa, the drain region being connected to the drift region.

3. The method of claim 2 further comprising: forming a source electrode connected to the source region; and

forming a drain electrode connected to the substrate.

4. The method of claim **1** wherein the dielectric material 45 and the field plates are formed with a reduced spacing between the field plates and the mesa near the body region as compared to near the lower portion of the mesa.

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- 5. The method of claim 1 wherein the first conductivity type is n-type.
- 6. The method of claim 1 wherein the mesa is formed with a doping concentration that is lower near the body region, as compared to the lower portion.
- 7. The method of claim 1 wherein the drift region has a linearly graded doping profile.
- **8**. The method of claim **1** wherein the dielectric material comprises silicon dioxide.
- 9. The method of claim 1 wherein the field plates comprise doped polysilicon.
- 10. A method for fabricating a high-voltage transistor comprising:

forming, in a semiconductor substrate of a first conductivity type, first and second trenches that define a mesa having respective first and second sidewalls;

partially filling each of the trenches with a dielectric material that covers the first and second sidewalls;

filling a remaining portion of the trenches with a conductive material to form first and second field plates in the first and second trenches, respectively, the first and second field plates extending vertically from near a bottom of the mesa to a top surface of the semiconductor substrate, each of the first and second field plates being respectively separated from the first and second sidewalls of the mesa by a distance of at least 2.0 µm;

forming source and body regions in an upper portion of the mesa, the source region being of the first conductivity type and the body region being of a second conductivity type opposite to the first conductivity type, the body region separating the source from a lower portion of the mesa, the lower portion of the mesa comprising a drift region; and

forming a gate embedded within the dielectric material adjacent the body region, the gate being insulated from the body region on one side, and from the first and second field plates on an opposite side.

11. The method of claim 10 further comprising:

forming a drain region of the first conductivity type at the bottom of the mesa, the drain region being connected to the drift region.

12. The method of claim **10** further comprising:

forming a source electrode connected to the source region and to the first and second field plates; and

forming a drain electrode connected to the substrate.

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